Harivallabh Ashok

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Objective

Aspiring VLSI Engineer with hands-on experience in RISC-V SoC integration and EDA automation at RISE Lab, IIT Madras. Seeking an 8th-semester project/internship at a leading semiconductor company to contribute to RTL design, functional verification, and SoC development.

Education

Amrita Vishwa Vidyapeetham Bangalore
B.Tech, ECE 6th Sem, CGPA – 7.58 *Aug 2023 — Present*

Internship

VLSI Design Intern – RISE Lab IIT Madras May 2026 – Jul 2026

- Developed and enhanced a Python- and YAML-based automation framework for SoC peripheral integration, eliminating manual backend configuration.
- Debugged and resolved peripheral and SoC integration issues, validated designs by generating FPGA bitstreams, and verified functionality on the Nexys Video FPGA board.
- Built and validated multiple reusable peripheral configurations for deployment, improving the scalability and reliability of the SoC peripheral integration framework.

Projects

Low-Cost VLSI Sorting Architectures Sep 2025 — Apr 2026

- Designed folded and parallel sorter architectures to achieve low cost and high throughput
- Developed RTL and testbench code for functional verification
- Implemented using FPGA hardware to evaluate real-world cost and performance and integrated with input and output sensors for seismic activity detection

System APB-Based SPI Interface Design and Verification Apr 2026 — Apr 2026

- Designed an APB-based SPI Master Interface in Verilog, implementing baud rate generation, shift register, and slave select logic.
- Developed a layered SystemVerilog testbench with generator, driver, monitor, scoreboard, and functional coverage.
- Debugged SPI timing, clock synchronization, and serial data alignment using waveform analysis.

AI Image and Video Classification System Jan 2025 — Apr 2025

- Developed a project using a deep learning model to distinguish between AI-generated and human-made images and videos with 90 percent accuracy.
- Designed and trained a CNN–Decision Tree model for AI vs. real image/video classification.
- Built a local server-based web application for the model using Python (Flask) and JavaScript

Certifications

- **MAVEN Silicon**, Bangalore - VLSI Design course July 2025-Present

Skills

- **HDLs**: Verilog, SysVerilog
- **Tools**: Vivado, Xilinx ISE, LTspice, Keil Microvision 4, Proteus, Arduino
- **Programming Languages**: Python, Embedded C(Intermediate), Java
- **Expertise**: VLSI, Embedded Systems, Deep learning